AN EQUIVALENT CIRCUIT MODEL OF A PLATED-THROUGH-HOLE INTERCONNECT FOR MULTILAYER STRIPLINE CIRCUITS

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Abstract

An empirically-based equivalent circuit model of a plated-through-hole (PTH) interconnect for multilayer stripline circuits is presented. The model, a distributed network of lumped components whose values are functions of the geometry of the interconnect, was based on the time domain analysis of extensive empirical data. The measured data were taken from a multilayer stripline test fixture containing 132 different interconnect architectures. The model provides an accurate characterization of the interconnect impedance from 0.045 to approximately 14 GHz. General design guidelines, based on observations of the physical range of configurations studied, are also presented.

Introduction

The plated-through-hole (PTH) interconnect provides a low-cost alternative for internal connections between adjacent layers in a multilayer stripline assembly. Such internal connections facilitate the three dimensional integration of stripline circuits, making it possible to reduce circuit weight, volume, and cost. Previously, no predictive or theoretical analysis of such interconnects existed, and the interconnects were individually developed at significant cost. The present model is intended to predict the impedance of the interconnect at microwave frequencies, so that implementations can be designed rapidly, efficiently, and at lower cost. The ability to predict interconnect performance will prove valuable in a wide range of future applications as microwave circuits demand higher level integration and as digital clock frequencies approach 1 GHz.

The approach taken for this study was to develop a test fixture that would provide a large quantity of empirical data from which a model would be derived. A base-line interconnect design was postulated, using a model for coaxial transmission line as the first approximation [1]. Physical parameters and the range over which they could be varied were identified. An experiment method was implemented to minimize the number of tests yet maximize the quality of the measured data. Microwave measurements were made from 0.045 to 18.045 GHz, and the interconnect impedances were de-embedded from their stripline feed circuits. Specific equivalent circuit models, based on time domain analysis of the empirical data, were constructed for a majority of the interconnects. A general model was then developed through statistical analysis of the specific models.

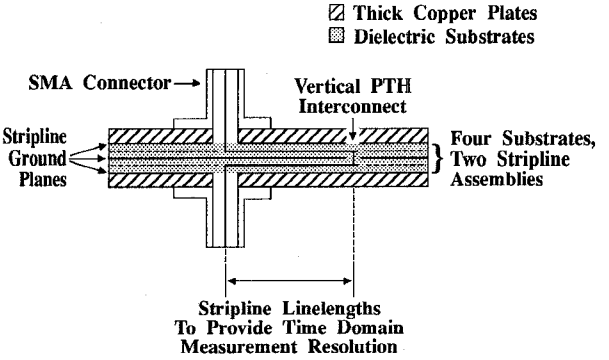

Figure 1. Cross-sectional view of the interconnect test fixture.

Experiment Design

The interconnect test fixture, whose cross-section is detailed in Figure 1, contained two stripline assemblies bonded together with a common ground plane. The four substrates (two per stripline assembly) were each 0.020 inch thick Rogers RT/duroid 6002, with a relative permittivity (ε_r) of 2.94. The stripline substrate material properties and ground plane spacing were held constant throughout the experiment. The effect of variation of five machined and plated features of the interconnect architecture was investigated. The five architectural parameters, shown in Figure 2, were: the PTH diameter (HD), the plated mode suppression arc inner radius (AR), the PTH support metallization ring radius (or via pad, VP), the plated mode suppression arc inner support metallization radius (MP), and the ground plane PTH support metallization radius (GP). The physical dimensions investigated and a description of the nomenclature used to represent the interconnect configurations are shown in Figure 3. (A number enclosed in parentheses within a test name signifies that the feature size was not of the standard set listed in Figure 3. The number in parentheses specifies the non-standard feature size in inches.) To reduce the number of interconnect tests while maintaining the quality of the experiment, a $\frac{1}{9}$ 3^5 fractional factorial experiment method was implemented [2]. The fractional factorial experiment set specified 81 configurations, which were used to provide the empirical data for the model development. 51 additional parametric and extreme-value tests were constructed for model verification.

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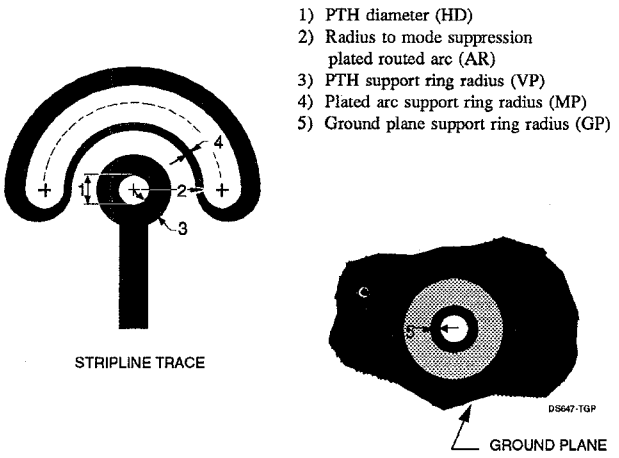

Figure 2. Circuit trace and ground plane view of the five PTH architectural parameters investigated.

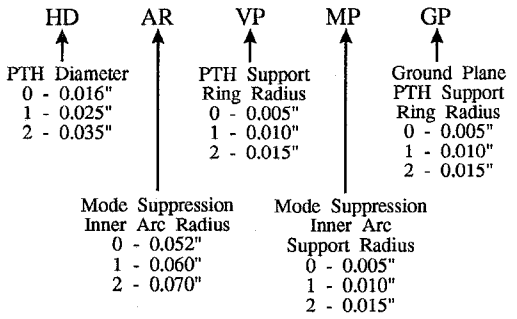

Figure 3. Interconnect nomenclature and physical dimensions.

Equivalent Circuit Model

The equivalent circuit model was based on the time domain analysis of the de-embedded PTH interconnects. It was noted from the interconnect low-pass time domain responses that a network of five distributed, lumped components could provide an accurate model. The equivalent circuit model of the PTH interconnect is shown in Figure 4. The capacitor should be located at the ground plane at the midpoint of the PTH. Specific models with fixed-valued components were generated for the 81 interconnects in the fractional factorial test set. Statistical analysis was performed on the fixed component values to develop linear regression models for the five component variable reactances (L_1, L_2, C, L_3, and L_4), as shown in Equation 1. The tabulated variable coefficients are included in Tables 1-3.

$$Reactance = V_{constant} + (1st\,Order) + (2nd\,Order) + (3rd\,Order) \quad (1)$$

where:

$$1st\,Order = V_{HD}\cdot HD + V_{AR}\cdot AR + V_{VP}\cdot VP + \ldots$$

$$2nd\,Order = V_{HD^2}\cdot HD^2 + V_{VPMP}\cdot VP\cdot MP + \ldots$$

$$3rd\,Order = V_{HD^3}\cdot HD^3 + V_{HDARVP}\cdot HD\cdot AR\cdot VP + V_{HD^2AR}\cdot HD^2\cdot AR + \ldots$$

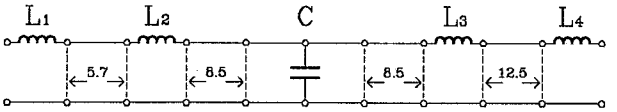

Figure 4. PTH interconnect equivalent circuit model (dimensions in millimeters).

Measurement Techniques and Impedance De-embedding

Each PTH interconnect was embedded within a stripline circuit and therefore was not directly accessible for measurement. Time domain reflectometry measurement and impedance de-embedding techniques were employed to separate the contribution of the interconnect from the overall circuit performance[3]. Time gated band-pass reflectometry measurements were completed for every interconnect and input connector pair from 0.045 to 18.045 GHz. The electrical phase delay through the broadside (90°) SMA connector was determined through the use of an embedded impedance standard. The measured data pairs, the phase delay to the impedance standard, and estimated transmission losses were used to de-embed the actual interconnect impedance.

Measured and Modeled Results

The empirical data revealed a wide range of interconnect performances. Figures 5, 6, and 7 present the frequency and time domain responses of three interconnects representative of the best, nominal, and worst performances observed. The frequency domain responses indicated that, although the low-frequency impedance was adequately matched, the high frequency impedance became quite reactive. The time domain responses provided insight into the types and distributed nature of the reactances required to formulate a suitable equivalent circuit model.

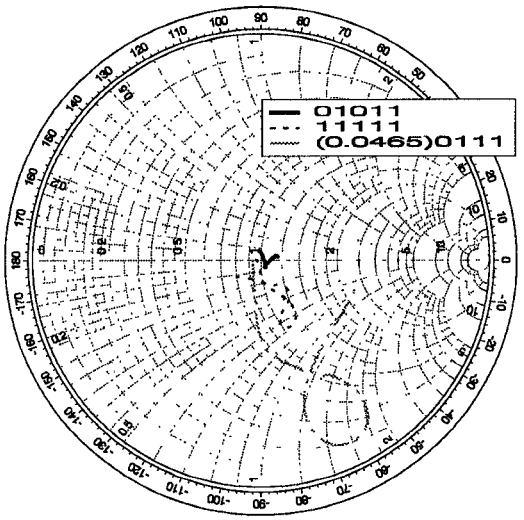

Figure 5. Frequency domain S_{11} impedance response for three interconnects.

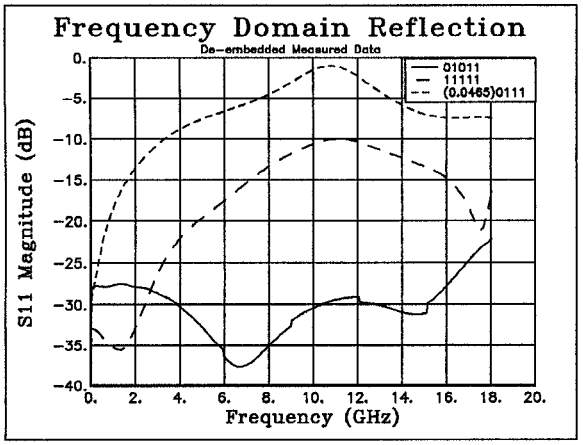

Figure 6. Frequency domain S_{11} response for three interconnects.

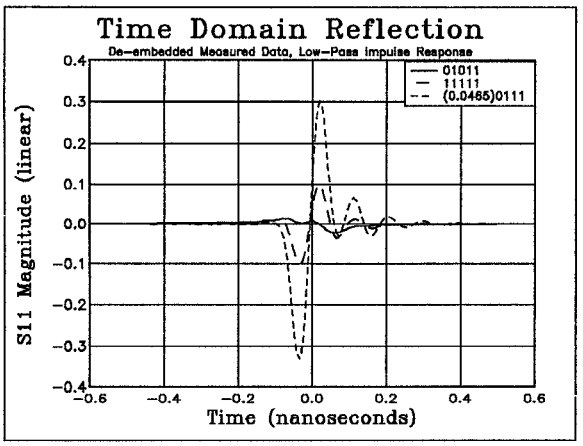

Figure 7. Time domain S_{11} response for three interconnects.

Figure 8 presents comparisons between measured and modeled results for interconnect configurations that were included in the fractional factorial test set. The model was based solely on the data from those 81 interconnects. Figure 9 presents comparisons between measured and modeled results for interconnects not included in the model development. Figure 9 also shows that the model has some utility for architectures outside the range of those used in the model development. (Interconnect (0.043)0111, whose response is presented in Figure 9, had a PTH diameter of 0.043 inch, yet the largest diameter used for the model development was 0.035 inch.)

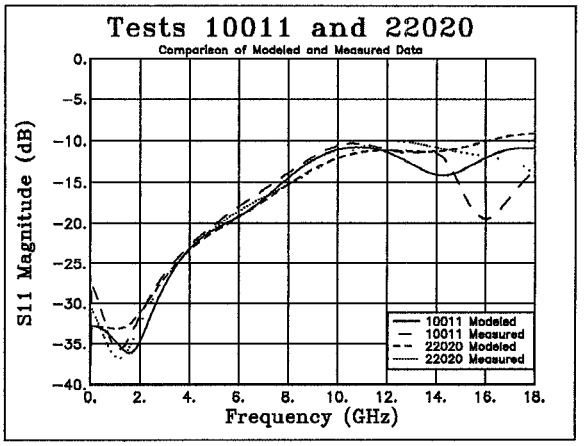

Figure 8. Comparison of modeled and measured data for interconnects 10011 and 22020.

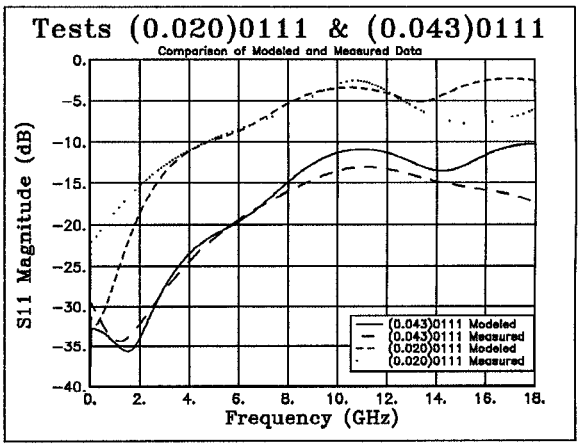

Figure 9. Comparison of modeled and measured data for interconnects (0.020)0111 and (0.043)0111. Note that these interconnects were not used in the model development.

Results and Conclusions

The equivalent circuit model can predict the impedance of the PTH interconnect within a range of physical configurations. The predicted performance was accurate for the 0.045 to 14 GHz range. Above 14 GHz, the model did not match the measured results. The frequency windowing technique used for the time domain measurement sidelobe suppression is believed to be the primary contributor to the high frequency inaccuracy.

Although the following design guidelines were derived from a specific family of PTH interconnect geometries, these conclusions should prove useful for future interconnect implementations. As design rules-of-thumb, the interconnects performed acceptably well when:

1) PTH diameter $\leq 0.04\ \lambda_{dielectric}$
2) PTH support metallization ring radius $< 0.02\ \lambda_{dielectric}$
3) mode suppression arc inner radius $< 0.12\ \lambda_{dielectric}$
4) mode suppression arc inner support metallization radius $< 0.02\ \lambda_{dielectric}$
5) ground plane PTH support metallization ring radius $< 0.02\ \lambda_{dielectric}$.

Table 1. First Order Effect Variable Coefficients

Coeff.	L_1	L_2	C	L_3	L_4
V_{HD}	16.738	26.665	10.983	-223.89	-2.5985
V_{AR}	-78.801	-74.874	-4.5940	-111.03	-31.912
V_{VP}	-198.02	-195.15	13.522	-1125.0	4.2038
V_{MP}	-229.08	-214.26	2.2006	-478.43	-13.039
V_{GP}	-84.525	-80.858	4.4170	2015.3	-7.3857
$V_{constant}$	2.7149	2.5654	-.0448	3.8574	1.1801

Table 2. Second Order Variable Coefficients

Coeff.	L_1	L_2	C	L_3	L_4
V_{HD}^2	861.01	1282.2	-646.49	644.59	-674.87
V_{AR}^2	1728.4	1845.2	181.20	-1040.5	-327.76
V_{VP}^2	25179.	25544.	-900.48	111570.	-2825.8
V_{MP}^2	31069.	28872.	1753.1	51461.	5401.5
V_{GP}^2	6456.8	7081.4	23105.	-242906.	-17774.
V_{HDAR}	-1142.6	-1977.5	856.51	7800.8	1043.4
V_{HDVP}	185.99	63.197	1085.2	956.76	2086.4
V_{HDMP}	-60.049	500.12	-1652.3	-3758.1	-3535.1
V_{HDGP}	-160.92	239.82	-2172.9	-3166.6	-1541.1
V_{ARVP}	-1172.4	-1115.2	168.46	2434.6	-103.19
V_{ARMP}	-1822.6	-1502.8	295.09	969.01	416.42
V_{ARGP}	1088.1	332.22	-5603.4	7694.3	5695.8
V_{VPMP}	225.17	-2161.9	-1607.8	-1228.6	-3171.6
V_{VPGP}	-465.85	543.47	-2031.4	1530.2	920.58

Table 3. Third Order Variable Coefficients

Coeff.	L_1	L_2	C	L_3	L_4
V_{HD}^3	-5342.7	-10598.	8594.8	8183.1	13648.
V_{AR}^3	-11779.	-13564.	-2598.1	17033.	4544.5
V_{VP}^3	-798864.	-803394.	101791.	-3576605.	130246.
V_{MP}^3	-1007178.	-896010.	-12210.	-1331530.	-70169.
V_{GP}^3	-204984.	-151713.	-837131.	8211007.	688958.
V_{HDARVP}	10244.	20273.	-24532.	77700.	34011.
V_{HDARMP}	2513.6	-19354.	8840.6	59844.	28386.
V_{HDARGP}	2762.9	21454.	-1396.6	-56526.	-23683.
V_{HDVPMP}	-5997.7	3113.0	24208.	-117042.	-49876.
V_{HDVPGP}	9586.7	6901.1	28324.	176189.	60398.
V_{HDMPGP}	2898.1	-5920.0	29057.	47695.	-19465.
V_{ARMPGP}	-2397.8	-407.47	-3403.0	22398.	38359.
V_{VPMPGP}	346.10	-3414.3	-53460.	-242939.	-228104.
V_{ARVPGP}	-1698.8	-12642.	-10769.	-69829.	-44115.
$V_{HD}^2{}_{AR}$	-5127.3	-3897.4	-4979.3	-33557.	-10071.
V_{HDAR}^2	9648.0	15059	-4121.2	-54746.	-6997.0
$V_{HD}^2{}_{VP}$	-11434.	-27310.	7811.3	-44940.	-47228.
V_{HDVP}^2	-13489.	1.9893	351.24	-193072.	-76472.
$V_{HD}^2{}_{MP}$	-5234.0	9610.5	13288.	32732.	34112.
V_{HDMP}^2	12039.	14611.	-4779.3	-32842.	37644.
$V_{HD}^2{}_{GP}$	-3358.6	-9963.9	16871	79875.	34940.
V_{HDGP}^2	265.22	-47567.	423376.	5840.8	52451.
$V_{AR}^2{}_{VP}$	9153.3	10312.	9839.3	-27737.	-5152.2
V_{ARVP}^2	-11453.	-33160.	-41561.	2607.6	13773.
$V_{AR}^2{}_{MP}$	17433.	24762.	-11.953	18930.	10696.
V_{ARMP}^2	-20839.	-56053.	-23304.	-230082.	-127115.
$V_{AR}^2{}_{GP}$	-7311.3	-2324.7	43590.	-35696.	-27500.
V_{ARGP}^2	-12099.	-23965.	8195.0	-67263.	-83624.
$V_{VP}^2{}_{MP}$	-10456.	16278.	24025.	-70648.	-54707.
V_{VPMP}^2	11893.	93627.	39112.	383662.	375462.
$V_{VP}^2{}_{GP}$	-2699.9	41276.	54373.	51927.	62764.
V_{VPGP}^2	23480.	-20141.	71492.	40736.	117890.

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[3] Izadian, J. S. and S. M., *Microwave Transition Design*, Artech House, Norwood MA, 1988, pp. 101.